ABSTRACT

A data processing device is provided with an indexed-immediate addressing mode for processing streams of data. An instruction register 900 receives an instruction for execution. Decoding circuitry 913 selects a register specified by a field in an instruction to provide an index value. An immediate field from the instruction is combined with the index value by multiplexor 910 to form an address which can be used to access a data value or to form a target address for a branch instruction. Mux control 915 parses the immediate value to determine how to combine the immediate value and the index value.